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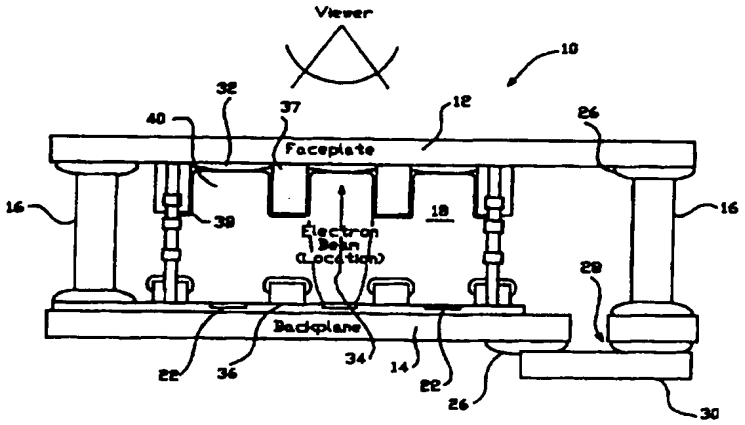

(57) Abstract

A field emission display device has a faceplate and a backplate. The faceplate includes a faceplate interior side with an active region made of a plurality of phosphor pixel elements; and the backplate has a backplate interior side with a plurality of field emitters. Sidewalls are positioned between the faceplate and the backplate, to form an enclosed sealed envelope between the sidewalls, backplate interior side and the faceplate interior side. At least one spacer wall in the envelope supports the backplate and the faceplate against forces acting in a direction toward the envelope. At least one internal structure fixes and constrains the faceplate and the backplate, and aligns a plurality of phosphor pixels with corresponding field emitters. Additonally, the faceplate can include at least one faceplate fiducial, and the backplate include a corresponding backplate fiducial. The faceplate fiductial is optically aligned with the backplate fiducial. First, the spacer wall is positioned in the wall gripper. The faceplate and backplate fiducials are then optically aligned, and the spacer wall then introduced into the locator. Phosphor pixels are aligned with their corresponding field emitters. There is no need for external fixturing devices in the high temperature bonding and sealing processes of the display.

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FIELD EMISSION DEVICE WITH INTERNAL STRUCTURE FOR ALIGNING PHOSPHOR PIXELS WITH CORRESPONDING FIELD EMITTERS

CROSS-REFERENCE TO RELATED APPLICATIONS

To the extent not repeated herein, the contents of Serial Nos. 08/188,856, filed January 29, 1994, 08/012,542, filed February 1, 1993 and U.S. Patent No. 5,424,605, all assigned to the same assignee as this application are incorporated by reference herein.

BACKGROUND

Field of the Invention

This invention relates generally to field emission devices, and more particularly, to field emission devices with at least one internal structure that includes fiducials to optically align the faceplate and the backplate, and at least one internal structure that fixes and constrains the faceplate and backplate to align a plurality of phosphor pixels with corresponding field emitters.

Description of the Related Art

Field emission devices include a faceplate, a backplate and connecting walls around the periphery of the faceplate and backplate, forming a sealed vacuum envelope. Generally in field emission devices, the envelope is held at vacuum pressure, which in the case of CRT displays is about 1×10^{-7} torr or less. The interior surface of the faceplate is coated with light emissive elements, such as phosphor or phosphor

patterns, which define an active region of the display. Cathodes, (field emitters) located adjacent to the backplate, are excited to release electrons which are accelerated toward the phosphor on the faceplate, striking the phosphor, and causing the phosphor to emit light seen by the viewer at the exterior of the faceplate. Emitted electrons for each of the sets of the cathodes are intended to strike only certain targeted phosphors. There is generally a one-to-one correspondence between each emitter and a phosphor.

Flat panel displays are used in applications where the form-factor of a flat display is required. These applications are typically where there are weight constraints and the space available for installation is limited, such as in aircraft or portable computers.

A certain level of color purity and contrast are needed in field emission devices. Contrast is the difference between dark and bright areas. The higher the contrast, the better. The parameters of resolution, color-purity and contrast in a flat cathodeluminescent display depend on the precise communication of a selected electron emitter with its corresponding phosphor pixels. Additionally, high picture brightness (lumens), requires either high power consumption or high phosphor efficiency (lumens/watt).

High power consumption in many applications is not desirable. Efficiency for many phosphors increases as the operating anode voltage increases; and the required operating brightness can be achieved with lower power consumption at high voltage, as illustrated in Figure 1. In order to satisfactorily operate at high anode voltages, e.g., 4 kV or higher, the backplate containing the emitter array must be spatially separated from the faceplate, containing the phosphor pixels, by a distance sufficient

to prevent unwanted electrical events between the two. This distance, depending on the quality of the vacuum and the topography of the substrates, is typically greater than about 2 mm.

With the constraints of faceplate and backplate glass area and thickness, the vacuum envelope is unable to withstand 1 atmosphere or greater external pressure without inclusion of the spacer walls. If the spacer walls are not included then the faceplate and backplate can collapse. In rectangular displays, having greater than approximately a 1 inch diagonal, the faceplate and backplate are particularly susceptible to this type of mechanical failure due to their high aspect ratio, which is defined as the larger dimension of the display divided by the thickness of the faceplate or backplate. The use of spacer walls in the interior of the field emission device substantially eliminates this mechanical failure.

The use of spacer walls has been reported in U.S. Patent No. 4,900,981; U.S. Patent No. 5,170,100; EPO 464 938 A1; EPO 436 997 A1; EPO 580 244 A1; and EPO 496 450 A1.

The faceplates and backplates for the desired flat, light portable display are typically about 1 mm thick. To avoid seeing the spacer walls at the exterior of the faceplate, the spacer walls should be hidden behind a suitable structure such as a black matrix.

Additionally, flat panel displays to date and standard CRT's have high-temperature assembly requirements, including but not limited to plasma addressed liquid crystal (PALC), and the like, where the alignment during assembly consists of external, mechanical alignment of the faceplate and the backplate so that the correspondence of the phosphor pixels and the associated cathode emitters are initially within tolerance. These external fixturing devices travel with the field emission display

through the required high temperature bonding and sealing processes. External fixturing devices have difficulties in maintaining a high precision of alignment because of differences in the coefficient of thermal expansion between the field emission display and the fixturing. Resulting misalignment gives a loss of color purity and resolution in the field emission display. Another disadvantage of external tooling is the cost of individual fixture tooling for each field emission display during the sealing and thermal processing of the displays.

It would be desirable to provide, (i) a field emission display which does not use external fixturing devices in the high temperature bonding and sealing processes, (ii) a faceplate for a field emission display that includes a black matrix grid, formed on the faceplate interior side and made of column and row guard bands, with a wall locator formed in a column or row guard, (iii) a self aligned focus grid for a field emission display, and (iv) in a high voltage display, a plurality of scattering shields, defining a subpixel volume, to reduce electron escape.

SUMMARY

Accordingly, it is an object of the invention to provide a field emission display device that does not use external fixturing devices during the high temperature bonding and sealing processes for aligning a plurality of phosphor pixels with corresponding field emitters.

Another object of the invention is to provide a faceplate for a field emission display that includes a black matrix formed on an interior surface of the faceplate, and a wall locator formed in the black matrix.

Yet another object of the invention to minimize misalignment of the electron beam in a field emission display and the consequential loss of color purity.

Still a further object of the invention is to provide a flat panel display with a faceplate interior side that includes a plurality of scattering shields surrounding each phosphor subpixel and defining a subpixel volume.

These and other objects are achieved in a field emission display device that includes a faceplate and a backplate. The faceplate has an interior side with an active region made of pluralities of phosphor pixel elements. The backplate has an interior side with pluralities of field emitters, each plurality of field emitters defining a sweet spot. Sidewalls are positioned between the faceplate and the backplate to form an enclosed sealed envelope between the sidewalls, backplate interior side and the faceplate interior side. At least one spacer wall is positioned in the envelope to support the backplate and the faceplate against forces acting in a direction toward the envelope. Further, at least one internal structure is included that fixes and constrains the faceplate and the backplate relative to each other, and aligns a phosphor pixels with corresponding field emitters.

The internal structure includes a spacer wall gripper with a receiving trench formed on the interior side of the faceplate, and a locator formed on the interior side of the backplate. The spacer wall is mounted in the receiving trench and is retained in the locator. The wall gripper has sufficient flexibility to receive the spacer wall in a substantially straightened geometry which is easily maintained throughout the sealing and thermal processing of the display. Each receiving trench has a trapezoid geometry which is very effective in gripping the spacer wall.

The width of the receiving trench is the same width or smaller than a width of the spacer wall.

The faceplate and backplate can each include an alignment fiducial. A spacer wall is positioned in the wall gripper. The faceplate and backplate fiducials are then optically aligned, and brought together so that the spacer wall becomes positioned in the locator. This essentially eliminates the need for external fixturing devices during the bonding and sealing stages, and the phosphor pixels are aligned with the corresponding field emitters .

One end of the spacer wall is fixably mounted in the receiving trench by the use of, for example, a frit. The spacer wall can have a different coefficient of thermal expansion than the faceplate or the backplate. This results because the receiving trench is able to grip and position the spacer walls even though there is a difference in thermal expansion of the faceplate, backplate and spacer walls during thermal and sealing processing.

DESCRIPTION OF THE DRAWINGS

Figure 1 is a graph of a curve of luminous efficiency verses voltage for a representative cathode luminescent phosphor.

Figure 2 is a perspective view of a field emission display device.

Figure 3 is a cross-sectional view of the field emission display device of Figure 2.

Figure 4 is a cross-sectional view of part of a flat panel display according to an embodiment of the invention including field emitters, phosphor subpixels, and scattering shields.

Figure 5 is a schematic diagram of back scattered electrons in a display without scattering shields

Figure 6 is a schematic diagram illustrating the effect of scattering shields and back scattered electrons.

Figure 7 is a graph of the fraction of current striking another phosphor subpixel verses the height of scattering shields for a typical display operated at 4 kV.

Figure 8 is an exploded view of the field emission device with fiducials formed in the black matrix and the focus grid.

Figure 9 is an exploded view of the field emission device with fiducials formed in the faceplate substrate and the focus grid.

Figure 10 is an enlarged perspective view of a spacer wall gripper formed at the interior side of the faceplate.

Figure 11 is a perspective view of the spacer wall gripper and the pluralities of phosphor pixels.

Figure 12 illustrates a perspective view, as in Figure 11, with the spacer wall being introduced into the receiving trench.

Figure 13 is a perspective view of the spacer wall positioned in the receiving trench formed in the black matrix.

Figure 14 is a perspective view of the faceplate interior side with spacer walls positioned in receiving trenches formed in the black matrix.

Figure 15 is a cross-sectional view of a wall spacer in a receiving trench, and illustrates that the receiving trench is flared with a trapezoid geometry.

Figure 16 illustrates a process for creating the wall gripper structure.

Figure 17 illustrates a process for creating a locator formed on the interior side of the backplate.

Figure 18 is a perspective view of the backplate.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

In the following description, embodiments of the invention are described with respect to a field emission device, more particularly, to a flat cathode ray tube display.

Herein, a flat panel display is a display in which a faceplate and backplate are substantially parallel, and the thickness of the display is small compared to the thickness of a conventional deflected-beam CRT display. The thickness of the display is measured in a direction substantially perpendicular to the faceplate and backplate. Often the thickness of a flat panel display is substantially less than about 2.0 inches, and in one embodiment it is about 4.5 to 7.0 mm.

Referring now to Figure 2, a flat panel display 10 includes a faceplate 12, backplate 14 and side walls 16, which together form a sealed envelope 18 that is held at vacuum pressure, e.g., approximately 1 x 10^{-7} torr or less. One or more spacer walls 20 support faceplate 12 against backplate 14. Spacer walls 20 can include electrodes positioned along their longitudinal length. For purposes of this disclosure, spacer walls 20 include walls, posts and wall segments.

Further, spacer walls 20 have a sufficiently small thickness so that they provide minimal interference with the operation of flat panel display 10, particularly the cathodes (field emitters) and phosphors of the device. Spacer walls 20 are made of a ceramic, glass, glass-ceramic, ceramic tape, ceramic reinforced glass, devitrified glass, amorphous glass in a

flexible matrix, metal with electrically insulating coating, bulk resistivity materials such as a titanium aluminum chromium oxide, high-temperature vacuum compatible polyimides or insulators such as silicon nitride. Spacer walls 20 have a thickness of about 20 to 60 μm, and a center-to-center spacing of about 8 to 10 mm. Spacer walls 20 provide internal supports for maintaining spacing between faceplate 12 and backplate 14 at a substantially uniform value across the entire active area of the display at an interior surface of faceplate 12.

A plurality of field emitters 22 are formed on a surface of backplate 14 within envelope 18. For purposes of this disclosure, field emitters 22 can include a plurality of field emitters or a single field emitter. Row and column electrodes control the emission of electrons from field emitters 22. The electrons are accelerated toward a phosphor coated interior surface of faceplate 12. Integrated circuit chips 24 include driving circuitry for controlling the voltage of the row and column electrodes so that the flow of electrons to faceplate 12 is regulated. Electrically conductive traces are used to electrically connect circuitry on chips 24 to the row and column electrodes.

Referring now to Figure 3, faceplate 12 and backplate 14 consist of glass that is about 1.1 mm thick. A hermetic seal 26 of solder glass, including but not limited to Owens-Illinois CV 120, attaches side walls 16 to faceplate 12 and backplate 14 to create sealed envelope 18. The solder glass must withstand a 450 degree C sealing temperature. Within envelope 18 the pressure is typically 10^{-6} torr or less. This high level of vacuum is achieved by evacuating envelope 18 through pump port 28 at high temperature to cause absorbed gasses to be removed from all

internal surfaces. Envelope 18 is then hermetically sealed by a pump port patch 30.

Faceplate 12 includes pluralities of pixels. In order to provide good purity of color and high resolution, electrons emitted by field emitters 22 are directed to, and fall only on a corresponding plurality of pixels. An electron beam 34 from field emitters 22 is focussed and directed by a focus grid 36 to a color picture element comprised of a plurality of phosphors 32, and a black matrix 37 formed on an interior side of faceplate 12.

Various parameters are associated with the direction of electrons from field emitters 22 to the proper associated plurality of phosphor pixels 32. These include, but are not limited to, (i) the precision of location of the field emitter 22 relative to focus grid 36, (ii) the precision of location of the plurality of phosphor pixels 32 relative to black matrix 37, and (iii) the alignment of focus grid 36 to black matrix 37. A light reflective layer, including but not limited to aluminum, is deposited on black matrix 37 and phosphor pixels 32 with a thickness of about 200 to 600Å.

The ratio of area of the plurality of phosphor pixels 32 to black matrix 37 for a 10 inch diameter screen with color resolution of 640(x3) x 480 picture elements is about 50%. The minimum width of black matrix 37 is therefore about 0.001 inches. This implies a maximum misalignment of electron beam 34 to the corresponding phosphor pixels 32 (from all contributors) to be less than half the maximum black matrix width (0.0005 inches) at any location of field emission device 10.

Field emission display 10 includes at least one internal structure in envelope 18 that fixes and constrains faceplate 12 to backplate 14, and thus aligns a plurality of phosphor pixels 32 with a corresponding sweet

spot associated with the field emitters 22 to within a predetermined tolerance of 0.0005 inches or less. This internal structure is a wall gripper 42 formed on an internal side of faceplate 12, and a locator 44 formed on an interior side of backplate 14. It will be appreciated that wall gripper 42 can be formed on back plate 14, and locator 44 can be formed on faceplate 12. A spacer wall 20 is mounted in wall gripper 42, and retained in locator 44. The most significant parameter of the alignment issue is the precision to which faceplate 12, e.g., black matrix 37 and phosphor pixels 32, is aligned to backplate 14, e.g., focus grid 36 and field emitters 22, and thereafter held in place without movement during the thermal assembly process. This is achieved with the internal structure in envelope 18 without the use of external fixturing devices.

Black matrix 37 is made of a photo-patternable material including but not limited to black chromium, polyimide, black frit, and the like. Both black matrix 37 and focus grid 36 are configured by photolithography. The phototooling to create black matrix 37 is substantially the same as the phototooling used to create focus grid 36, wall gripper 42 and locator 44.

Spacer walls 20 are first mounted in wall gripper 42. Thereafter, faceplate 12 and backplate 14 are locked together, to within the allowed tolerances, by positioning spacer walls 20 in corresponding locators 44.

Referring now to Figure 4, faceplate 12 and backplate 14 consist of glass that is about 1.1 mm thick. A hermetic seal 26 of solder glass, including but not limited to Owens-Illinois CV 120, attaches side walls 16 to faceplate 12 and backplate 14 to create sealed envelope 18. The entire display 10 must withstand a 450 degree C sealing temperature. Within envelope 18 the pressure is typically 10^{-7} torr or less. This high level of vacuum is achieved by evacuating envelope 18 through pump port

28 at high temperature to cause absorbed gases to be removed from all internal surfaces. Envelope 18 is then sealed by a pump port patch 30.

Faceplate 12 includes a plurality of phosphor subpixels 32. Electrons defining an electron beam 34 are accelerated from a plurality of field emitters with energies in the range of 1kV to 10kV. Electron beam 34 is focused by focus grid 36 to strike a corresponding phosphor subpixel 32. There is a one-to-one correspondence between a set of field emitters 22, positioned within a section of focus grid 36, to a phosphor subpixel 32. Each phosphor subpixel 32 is surrounded by a plurality of scattering shields 38 which define a subpixel volume 40.

Figure 5 illustrates the results with a black matrix but without scattering shields 38. Electrons in electron beam 34 are accelerated from a plurality of field emitters 22 to strike their corresponding phosphor subpixels 32. Some of these electrons are back scattered from a phosphor subpixel or an adjacent area to an internal support 20 as represented by ray 35. Other electrons are back scattered and strike non-corresponding phosphor subpixels, as shown with ray 39. Back scattered electrons can strike other insulating elements in envelope 18. Back scattering electrons onto resistive surfaces, such as internal supports 20, affects the ratio of brightness to power of display 10 by limiting the amount of current that can be used. Further, the back scattering onto internal supports 20 limits the height of internal supports 20 and thus the high voltage. Back scattering of electrons to non-corresponding phosphor subpixels reduces contrast and color purity of display 10. A black matrix typically has a low aspect ratio. Additionally, it is difficult to make a structure with a sufficient aspect ratio to prevent electrons escaping from their subpixel volume 40.

In Figure 6 the effects of scattering shields 38 are illustrated. Back scattered electrons strike scattering shields 38, represented by rays 41 and 43, and do not leave their scattering shield volumes 40. They remain essentially captured in their scattering shield volumes 40. Alternatively, if back scattered electrons escape from their scattering shield volume 40 scattering shields 38 capture the back scattered electrons as in the case of ray 45, preventing them from striking non-corresponding phosphor subpixels.

Referring now to Figure 7, the fraction of current striking another phosphor subpixel is shown as a function of scattering shield 37 height. Preferably, scattering shield 38 height is 12 μm, 25 μm, 25 μm, 50μm, 75 μm, 100μm, or greater. However, the actual height and size will vary depending on dimensions of the display. Scattering shields 38 can have heights in the range of about 20 to 200 μm, 20 to 100 μm, and 50 to 100 μm, scattering shields 38 provide a fivefold improvement in contrast.

Scattering shields 38 can be made of a photo patternable material including but not limited to polyimide. At least a portion of scattering shields 38 can include a black matrix material.

Referring now to Figures 8 and 9, alignment of faceplate 12 and backplate 14 is achieved with optical alignment fiducials 45 and 47, which can be integral to the structure of black matrix 37 and focus grid 36 respectively. Additionally, masks for fiducials 45 and 47 are integral to the phototooling, creating a geometric relationship between fiducial 45 and black matrix 37, and fiducial 47 and focus grid 36. Optionally, fiducials 45 and 47 can be on each of the substrates of faceplate 12 and backplate 14 respectively and not part of black matrix 37. In any event, fiducials 45 and 47 provide optical alignment of faceplate 12 to backplate 14, and of field

emitters 22 to corresponding phosphor pixels 32. When fiducials 45 and 47 are in optical alignment, e.g., when collimated light falls on faceplate 12 which is transparent to the light, the image of faceplate alignment fiducial 45 is projected onto and maps to backplate fiducial 47. A shadow mask is provided to permit the passage of optical light through fiducials 45 and 47.

The mounted spacer walls 20 are physically strong and rigid enough to withstand atmospheric pressure, and maintain alignment of faceplate 12 and backplate 14 through the sealing and thermal processing of the display. The shape of wall gripper 42, as more fully described hereafter, is designed to grip spacer wall 20 tightly and retard its movement.

As shown in Figure 10 black matrix 37 comprises column and row guard bands. Wall gripper 42 is formed on black matrix 37. Preferably, wall gripper 42 is formed in a column or row guard band. Wall gripper 42 has a height of about 0.001 inches or greater. A second layer of black matrix 37(a) is formed to create wall gripper 42, which is essentially a pair of raised structures 42(a) and 42(b), creating a receiving trench 46 for spacer wall 20. Wall gripper 42 is formed in a generally perpendicular direction in relation to a series of column guard bands 48. Wall gripper 42 is not visible or distinguishable from a row guard band 51 not containing a wall gripper. When viewed at the exterior of faceplate 12, wall gripper 42 is not visible or distinguishable from row guard band 51, and thus has optical integrity. That is, the viewed footprint is the same for a row guard band 51 with a wall gripper 42 as that of a row guard band 51 without a wall gripper 42.

In Figure 11, a first layer of black matrix 37 is formed, and then a second layer of black matrix 37(a) is created. Second layer 40(a) creates

wall gripper 42, with the corresponding raised structures 42(a) and 42(b) defining a receiving trench 46. As illustrated, pluralities of phosphor pixels 32 are defined by black matrix 37 and second layer of black matrix 37(a). Figure 12 illustrates the introduction of a spacer wall 20 into receiving trench 46.

Figure 13 illustrates spacer wall 20 positioned in receiving trench 46. In Figure 14 a perspective view of an interior side of faceplate 12 shows black matrix 37 and five spacer walls 20 positioned in wall grippers 42.

The material forming wall gripper 42 is vacuum-compatible at processing temperatures in that it does not decompose or create gas contaminants. Processing temperatures are in the range of about 300 to 450 degrees C. Wall gripper 42 is sufficiently flexible (capable of local deformation) to permit spacer walls 20 to have greater thicknesses than receiving trench 46, and still be capable of insertion into receiving trench 46. Wall gripper 42 also provides a straightening effect on spacer walls 20. Wall gripper 42 is capable of sufficient local deformation to straighten spacer walls 20.

As shown in Figure 15 wall gripper 42 has a receiving trench 46 geometry with a narrower aperture at the point of receiving a spacer wall 20, than the bottom of receiving trench 46. In one embodiment, the depth of receiving trench 46 can be about 0.002 inches.

One embodiment of the process for forming wall gripper 42 is now described, with reference to Figure 16.

A preferred material for wall gripper 42 is a photodefinable polyimide, such as OCG Probimide 7020, or other similar polymers from DuPont, Hitachi and the like.

Black matrix 37 is created from black chromium and photopatterned by conventional lithography on faceplate 12. A first layer of Probimide 7020, denoted as 54, is deposited on black matrix 37 by conventional spin deposition at 750 RPM for 30 seconds. Faceplate 12 is then baked on a hot plate at 70 degrees C for 6 minutes, followed by 100 degrees C for twenty minutes, to drive off solvents.

A second layer of Probimide 7020, denoted as 56, is deposited and baked under the same conditions as layer 54. The soft baked Probimide 56 is then photoexposed with an exposure dose of 250 mJ/sq cm at 405 nm through a mask 58 in proximity to Probimide layer 56. Exposed Probimide layer 56 is then baked for 3 minutes at 100 degrees C, followed by a room temperature stabilization of 15 minutes. Probimide layer 56 at this time has an exposure energy profile that creates the trapezoid shape, illustrated in Figure 15, that imparts the gripping function of wall gripper 42.

The Probimide is then developed in OCG QZ3501 by a puddle/spray cycle: [3 minutes puddle/1 minute, spray--repeat 1X] followed by a solvent rinse (OCG QZ 3512) for 1 minute. The developed wall gripper 42 is then hard baked for 1 hour at 450 degrees C in a nitrogen atmosphere with a thermal ramp of 3 degrees C per minute.

Spacer walls 20 are then inserted into wall gripper 42 , as shown in Figure 13. As illustrated, the insertion axis is perpendicular to the plane of faceplate 12. Insertion can also be accomplished parallel to the plane of faceplate 12 (i.e. slide spacer wall 20 into receiving trench 46 from one end). Spacer wall 20 extends beyond black matrix 37 in an amount sufficient to secure one of its ends with solder glass 60 to substrate 12. Receiving trench 46 has one ore more flared ends to facilitate spacer wall 20 insertion.

Figure 13 shows spacer wall 20 in place with only one end secured by solder glass 60, or other high temperature adhesives. Other suitable adhesives include but are not limited to polyimide, and the like. Solder glass 60 can be, but is not limited to, OI CV 120. The assembly shown in Figure 14 is then baked for one hour at 450 degrees C to devitrify solder glass 60. A suitable oven ramp is 3 degrees C/minute. Securing one end of spacer wall 20 provides mechanical stability of spacer wall 20 for subsequent processing. Additionally, since there is differential expansion and contraction during thermal processing, when spacer walls 20 are secured or pinned at both ends buckling of spacer wall 20 results. Securing spacer wall 20 at only one end enables the use of materials with substantially different coefficients of thermal expansion for spacer walls 20, faceplate 12 and backplate 14, because all differential movement of spacer wall 20 is along the axis of receiving trench 46.

It will be appreciated that the present invention is not limited to the preceding example of a process cycle. The present invention can be created with various modifications of this process cycle.

As shown in Figure 8, spacer wall 20 is fixed and constrained by wall gripper 42 and locator 44, and then once faceplate 12 and backplate 14 are optically aligned, spacer wall 20 is fixed and constrained in locator 44. Backplate 14 of display 10 is constructed to provide correspondence of features with faceplate 12 so that field emitters 22 communicate with the corresponding plurality of phosphor pixels 32, and wall gripper 42 is in optical alignment with locator 44. Wall locator 44 is formed by phototooling compatible with the tooling set used to create wall gripper 42, black matrix 37 and focus grid 36. Focus grid 36 is self aligned to field emitters 22.

Consequently, faceplate 12 with spacer walls 20 attached, may be brought into proximity to backplate 14, and be manipulated in the (x,y,0) axes so as to bring spacer wall 20 into alignment with wall locator 44, and a respective plurality of phosphor pixels 32 into alignment with its corresponding sweet spot 36. Faceplate 12 may then be translated in the z axis to cause spacer wall 20 to insert into wall locator 44. This assembly provides precision of alignment in the (x,y,0) axis and is held and maintained in position by the mechanically rigid structure formed by spacer walls 20, wall gripper 42 and locator 44. This structure may then be transported through a standard cycle of high temperature sealing and evacuation. Solder-glass may be used in the sealing process. This is done by baking at 450 degrees C for one hour and using a 3 degree C/minute thermal ramp. The only fixturing required is to provide sufficient force to hold faceplate 12 and backplate 14 together to maintain contact. No external locating and aligning fixturing is required during thermal processing.

With reference now to Figures 17 and 18, a process for forming locator 44 on backplate 14 is illustrated beginning with backplate 14, row electrodes 50 and column electrode 49. Row and column metallization, together with gate oxide, electron emitter, gate metal (not shown), are formed on the interior surface of backplate 14.

A first layer 64 of OCG Probimide 7020 polyimide is deposited on backplate 14 to a dry thickness of 45 microns by conventional spinning means for 10 seconds at a spin speed of 750 rpm.

First layer 64 is soft baked in a two-step process for 6 minutes at a temperature of 79 degrees C followed by 10 minutes at 100 degrees C. It is then exposed through a photomask 68 to define a column focus

electrode 70. The exposure parameters are: UV light at wavelength from 350 to 450 nm for an exposure dose of 250 mJ/sq cm. The exposed pattern is then developed in OCG QZ 3501 developer for 3 minutes to form column focus electrode 70.

A second layer 72 of polyimide is deposited to a dry thickness of 20 microns and exposed through a second photomask 74 using the same exposure and development parameters as first layer 64, to form row focus electrode 76 and locator 44. Locator 44 has a depth of about 10μm.

The polyimide is imidized by baking at a temperature of 460 degrees C in a nitrogen atmosphere for 1 hour.

Backplate structure includes electrically insulating backplate, a base electrode, an electrically insulating layer, metallic gate electrodes, field emitters positioned in gate electrodes, and focusing ridges positioned adjacent to gate electrodes.

The gate electrode lies on the insulating layer. The gate electrode is in the shape of a strip running perpendicular to the base electrode.

Field emitters contact the base electrode and extend through apertures in the insulating layer. The tips, or upper ends, of field emitters are exposed through corresponding openings in the gate electrode. Field emitters can have various shapes, including but not limited to cones, filament structures, and the like. Focusing ridges generally extend to a considerably greater height above the insulating layer than the a gate electrode. Preferably, the average height of focusing ridges is at least ten times the average height of a gate electrode. Typically, the height of focussing ridges is about 20 to 50 μm.

Field emitters emit electrons at off-normal emission angles when a gate electrode is provided with a suitably positive voltage relative to the

field emitter voltage. Emitted electrons move towards phosphor pixels. When struck by these electrons, phosphor pixels emit light.

Focusing ridges influence trajectories in such a way that the one-to-one correspondence of phosphor pixels to field emitters is maintained. The phosphors are struck by substantially all of the emitted electrons.

The height of scattering shields 38 is sufficient to reduce the number of scattered electrons which escape from a subpixel volume 40.

The foregoing description of preferred embodiments of the present invention has been provided for the purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise forms disclosed. Obviously, many modifications and variations will be apparent to practitioners skilled in this art. The embodiments were chosen and described in order to best explain the principles of the invention and its practical application, thereby enabling others skilled in the art to understand the invention for various embodiments and with various modifications as are suited to the particular use contemplated. It is intended that the scope of the invention be defined by the following claims and their equivalents.

What is claimed is:

1. A field emission display device, comprising:

a faceplate including a faceplate interior side with an active region made of a plurality of phosphor pixels;

a backplate including a backplate interior side with a plurality of field emitters;

sidewalls positioned between the faceplate and the backplate to form an enclosed sealed envelope between the sidewalls, backplate interior side and the faceplate interior side;

at least one spacer wall in the envelope supporting the backplate and the faceplate against forces acting in a direction toward the envelope; and

at least one internal structure that fixes and constrains the faceplate and the backplate, and aligns a plurality of phosphor pixels with corresponding field emitters.

2. The field emission display device of claim 1, wherein the internal structure includes, a spacer wall gripper.

3. The field emission display device of claim 2 wherein the spacer wall gripper includes a receiving trench formed on the interior side of the faceplate.

4. The field emission display device 3, wherein the internal structure includes, a locator formed on the interior side of the backplate.

5. The field emission display of claim 4, wherein the internal structure includes the spacer wall mounted at the interior side of the faceplate in the receiving trench, and retained in the locator at the interior side of the backplate.

6. The field emission display of claim 1, including a black matrix grid positioned adjacent to the faceplate interior side, the black matrix grid including the internal structure and a receiving trench that receives the spacer wall and mounts it relative to the plurality of phosphor pixels.

7. The field emission device of claim 6, wherein the black matrix is made of a photo patternable material.

8. The field emission device of claim 6, wherein the photo patternable material is polyamide.

9. The field emission device of claim 6, wherein one end of the spacer wall is fixably mounted to the faceplate.

10. The field emission device of claim 6, wherein the receiving trench straightens the spacer wall.

11. The field emission device of claim 6, wherein the spacer wall is substantially optically invisible to a viewer when viewed at an exterior surface of the faceplate.

12. The field emission device of claim 6, wherein the receiving trench has a first end that is closer to the faceplate interior side than a second end, and the second end is flared inward relative to the first end.

13. The field emission device of claim 12, wherein the receiving trench has a width that is the same or smaller than a width of the spacer wall.

14. The field emission display device of claim 1, wherein the spacer wall has a different coefficient of thermal expansion than a coefficient of thermal expansion of the faceplate.

15. The field emission display device of claim 1, wherein the internal structure includes a spacer wall gripper formed on the interior side of the backplate and a locator at the interior side of the faceplate.

16. The field emission display of claim 1, further including an alignment fiducial.

17. A backplate structure for a field emission display, comprising:

a transparent backplate substrate;

at least two opaque electrodes;

a plurality of transparent electrodes that are orthogonal to the opaque electrodes;

a plurality of field emitters formed on the opaque electrodes;

a focusing grid including an exterior surface and an electrically conductive layer positioned substantially over the exterior surface, the focusing grid being aligned to the opaque electrodes and transparent electrodes and electrically isolated from the transparent electrodes and the opaque electrodes.

18. The field emission display of claim 17, wherein the focusing grid includes a spacer wall gripper with a receiving trench adapted to receive a spacer wall.

19. A field emission display, comprising:

a faceplate substrate defining a faceplate interior side;

a plurality of phosphor pixels disposed on the faceplate interior side;

a transparent backplate substrate;

sidewalls combined with the faceplate substrate and the backplate substrate defining a display interior envelope that can be held at a vacuum;

a plurality of opaque electrodes;

a plurality of transparent electrodes that are orthogonal to the opaque electrodes;

a plurality of field emitters formed on the transparent electrodes;

a focusing electrode including an exterior surface and an electrically conductive layer positioned substantially over the exterior surface, the focusing electrode being aligned to the transparent electrodes and electrically isolated from the transparent electrodes and the opaque electrodes; and

driver circuitry supplying current to the display.

20. The display of claim 19 further comprising:

a plurality of spacer wall locators formed on an interior side of the backplate;

a plurality of deformable ribs positioned in the wall locators in a direction orthogonal to the wall locators.

21. The display of claim 19, wherein the transparent electrodes include opaque sections.

22. The display of claim 21, wherein the plurality of field emitters are formed on the opaque sections of the transparent electrodes.

23. A method for forming a backplate structure for a field emission device, comprising:

providing a backplate with an exterior surface and an internal surface, the backplate including a transparent substrate, a plurality of opaque electrodes, and an active area defined by a plurality of field emitters formed on the opaque electrodes;

applying a photo patternable material to substantially the entire internal surface;

creating a deformable wall locator by differential exposure of a row focus pattern and a column focus pattern of the internal surface to UV radiation through the exterior surface;

developing and curing the photo patternable material to form a cured photo patternable material with a row focus pattern of height h_1 and a column focus pattern of height h_2;

coating the cured photo patternable material with a conductive layer; and

creating a focusing electrode that is electrically isolated from the opaque electrodes.

24. The method of claim 23, wherein h_1 is less than, or equal to h_2.

25. The method of claim 23, wherein h_1 is greater than, or equal to h_2.

26. A faceplate of a field emission display, comprising:

a substrate defining a faceplate interior side;

a plurality of phosphor pixels disposed on the faceplate interior side;

a black matrix grid formed of a plurality of column and row guard bands on the faceplate interior side; and

a wall gripper formed in a column or row guard band, the wall gripper adapted to receive a spacer wall and mount it relative to the pluralities of phosphor pixels.

27. The faceplate of claim 26, wherein the spacer wall is positioned in the wall gripper and mounted relative to a corresponding locator formed on a backplate interior side.

28. The faceplate of claim 26, wherein the wall gripper includes a receiving trench.

29. The faceplate of claim 26, wherein the receiving trench is positioned adjacent to a plurality of deformation accommodation gaps.

30. The faceplate of claim 26, wherein the black matrix is made of a photo patternable material.

31. The faceplate of claim 26, wherein the black matrix is made of polyamide.

32. The faceplate of claim 26, wherein one end of the spacer wall is fixably mounted to the faceplate substrate.

33. The faceplate of claim 26, wherein a spacer wall is straightened in the receiving trench.

34. The faceplate of claim 26, wherein a spacer wall in the receiving trench is substantially optically invisible to a viewer when viewed at an exterior surface of the faceplate.

35. The faceplate of claim 26, wherein the receiving trench has a first edge that is closer to the faceplate interior side than a second edge, and the second edge is flared inward relative to the first end.

36. The faceplate of claim 26, wherein the receiving trench has a first end that is flared.

37. The faceplate of claim 26, wherein the receiving trench has a first end and a second end that are flared.

38. The faceplate of claim 31, wherein the faceplate fiducial is formed in the black matrix.

39. A flat panel display, comprising:

a faceplate including a faceplate interior side;

a backplate including a backplate interior side in an opposing relationship to the faceplate interior side;

side walls positioned between the faceplate and the backplate to form an enclosed sealed envelope between the side walls, backplate interior side and the faceplate interior side;

a plurality of phosphor subpixels positioned at the faceplate interior side;

a plurality of field emitters that emit electrons which are directed to a corresponding subpixel; and

a plurality of scattering shields surrounding each subpixel and defining a subpixel area, the scattering shields reducing a number of scattered electrons in the subpixel area from escaping from the subpixel area, wherein the height of the scattering shields surrounding a subpixel is sufficient to reduce the number of scattered electrons from exiting from their corresponding subpixel area and strike an incorrect subpixel.

40. The display of claim 39, wherein the height of the scattering shields surrounding a subpixel is sufficient to reduce the number of scattered electrons from exiting from their corresponding subpixel area and charge an insulating surface in the envelope.

41. The display of claim 39, wherein a voltage equal to or greater than 5kV is applied between the backplate and the faceplate.

42. The display of claim 39, wherein a voltage equal to or greater than 7kV is applied between the backplate and the faceplate.

43. The display of claim 39, wherein a voltage applied between the backplate and the faceplate is about 10kV.

44. A flat panel display, comprising:

a faceplate including a faceplate interior side;

a backplate including a backplate interior side in an opposing relationship to the faceplate interior side;

side walls positioned between the faceplate and the backplate to form an enclosed sealed envelope between the side walls, backplate interior side and the faceplate interior side, the faceplate, backplate and side walls defining a display envelope with at least one internal support;

a plurality of phosphor subpixels positioned at the faceplate interior side;

a plurality of field emitters that emit electrons which are directed to a corresponding subpixel;

a plurality of scattering shields surrounding each subpixel and defining a subpixel area, the scattering shields reducing a number of scattered electrons in the subpixel area from escaping from the subpixel area, wherein the height of the scattering shields surrounding a subpixel is sufficient to reduce the number of scattered electrons from exiting from their corresponding subpixel area and charge an internal insulating surface in the envelope; and

a locating groove formed in a column or row guard band, the locating groove adapted to receive an internal support and mount it relative to the phosphor subpixels.

45. The display of claim 44, wherein the height of the scattering shields surrounding a subpixel is sufficient to reduce the number of scattered electrons exiting from their corresponding subpixel area and strike a non-corresponding subpixel.

46. The display of claim 44, wherein the height of the scattering shields is about 20 to 200 μm beyond a height of the phosphor subpixels.

47. The display of claim 44, wherein the height of the scattering shields is about 20 to 100 μm beyond a height of the phosphor subpixels.

48. The display of claim 44, wherein the phosphor subpixels have a height that extends about 1 to 30 μm from the faceplate interior side into the envelope.

49. The flat panel display of claim 48, wherein the scattering shields have a height of about 12 μm extending beyond the phosphor subpixels.

50. The flat panel display of claim 48, wherein the scattering shields have a height of about 25 μm extending beyond the phosphor subpixels.

51. The flat panel display of claim 48, wherein the scattering shields have a height of about 50 μm extending beyond the phosphor subpixels.

52. The flat panel display of claim 48, wherein the scattering shields have a height of about 75 μm extending beyond the phosphor subpixels.

53. The flat panel display of claim 48, wherein the scattering shields have a height of about 100 μm extending beyond the phosphor subpixels.

54. The display of claim 44, further comprising:

at least one internal support in the envelope supporting the backplate and the faceplate against forces acting in a direction toward the envelope.

55. The display of claim 44, wherein the scattering shields surrounding a subpixel are of sufficient height to reduce the number of

scattered electrons from their corresponding subpixel area and charge the internal support.

56. The display of claim 44, wherein the scattering shields are made of a material selected from the group consisting of polyamide, metal, glass and ceramic.

57. The display of claim 44, wherein a scattering shield glass interface made of an optically absorbing material.

58. The display of claim 44, wherein a voltage equal to or greater than 1kV is applied between the backplate and the faceplate.

59. The display of claim 44, wherein a voltage equal to or greater than 3kV is applied between the backplate and the faceplate.

60. The display of claim 44, wherein a voltage equal to or greater than 5kV is applied between the backplate and the faceplate.

61. The display of claim 44, wherein a voltage equal to or greater than 7kV is applied between the backplate and the faceplate.

62. The display of claim 44, wherein a voltage applied between the backplate and the faceplate is about 10kV.

63. A method for forming a backplate structure for a field emission device, comprising:

providing a backplate with an exterior surface and an internal surface, the backplate including a transparent substrate, a plurality of opaque electrodes, a plurality of transparent electrodes that are orthogonal to the opaque electrodes, and a plurality of field emitters formed on the opaque electrodes;

applying a photo patternable material to substantially the entire internal surface;

exposing the internal surface to UV radiation through the exterior surface;

developing and curing the photo patternable material to form a cured photo patternable material;

coating the cured photo patternable material with a conductive layer; and

creating a focusing electrode electrically isolated from the opaque electrodes and aligned to the plurality of opaque electrodes.

64. The method of claim 63,. further comprising:

exposing the internal surface to UV radiation through a mask onto an internal side of a backplate substrate.

65. The method of claim 63, wherein the conductive layer is a metal layer.

66. The method of claim 63, wherein the focusing electrode is created by baking the backplate.

67. The method of claim 63, wherein the conductive layer is a metal layer.

68. The method of claim 63, wherein the focusing electrode is created by backing the backplate.

69. A method for forming a backplate structure for a field emission device, comprising:

providing a backplate with an exterior surface and an internal surface, the backplate including a transparent substrate, a plurality of opaque electrodes, and an active area defined by a plurality of field emitters formed on the opaque electrodes;

applying a photo patternable material to at least the active area;

exposing the internal surface to UV radiation through the exterior surface;

developing and curing the photo patternable material to form a cured photo patternable material;

coating the cured photo patternable material with a conductive layer; and

creating a focusing grid that is electrically isolated from the electrodes.

70. The method of claim 69, wherein the focusing electrode is created by backing the backplate.

71. The method of claim 69, wherein the focusing electrode is created by baking the backplate.

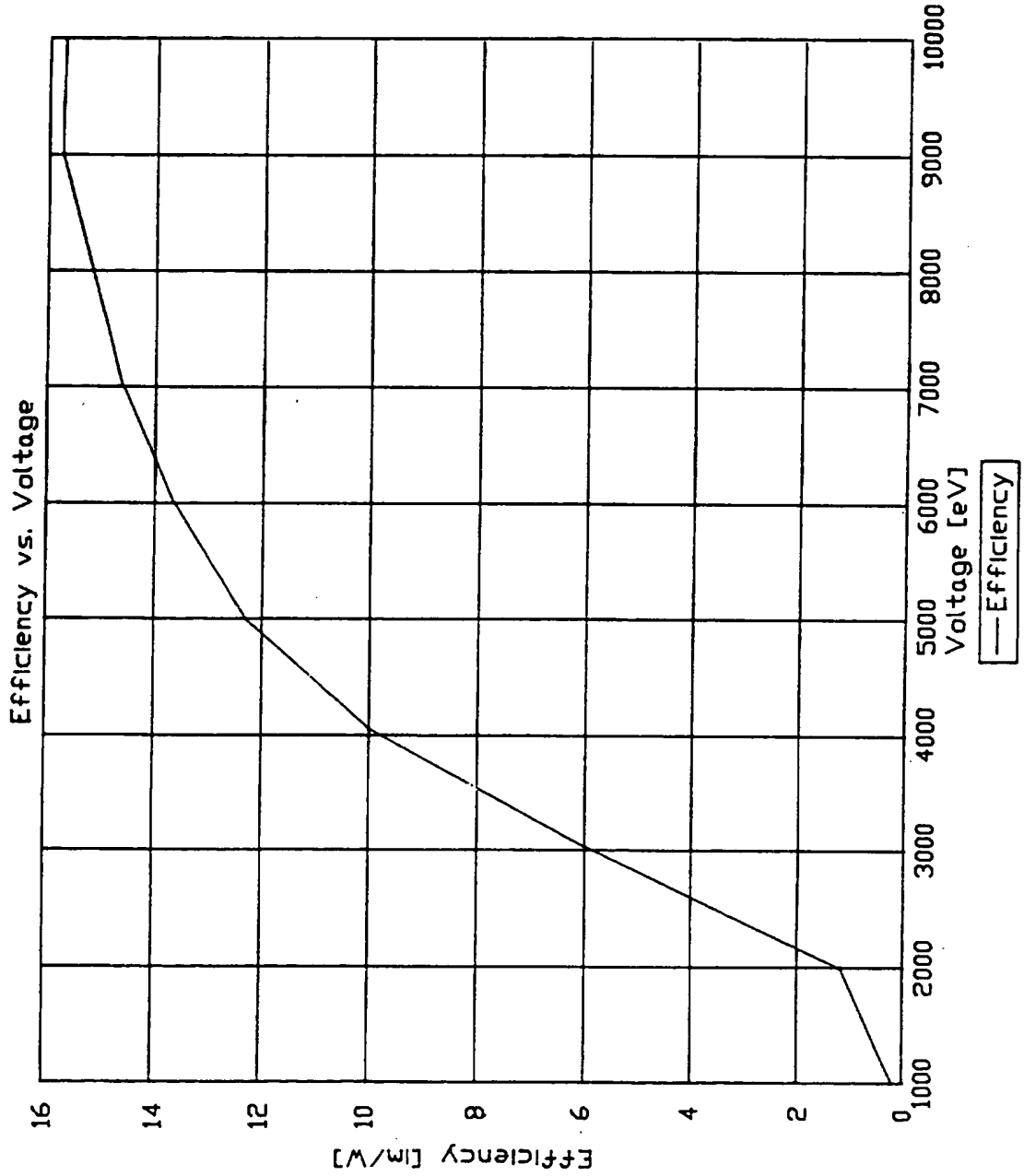

Efficiency vs. Voltage
Efficiency [lm/W]
0
2
4
6
8
10
12
14
16
1000
2000
3000
4000
5000
6000
7000
8000
9000
10000
Voltage [eV]
Efficiency

FIG. 1

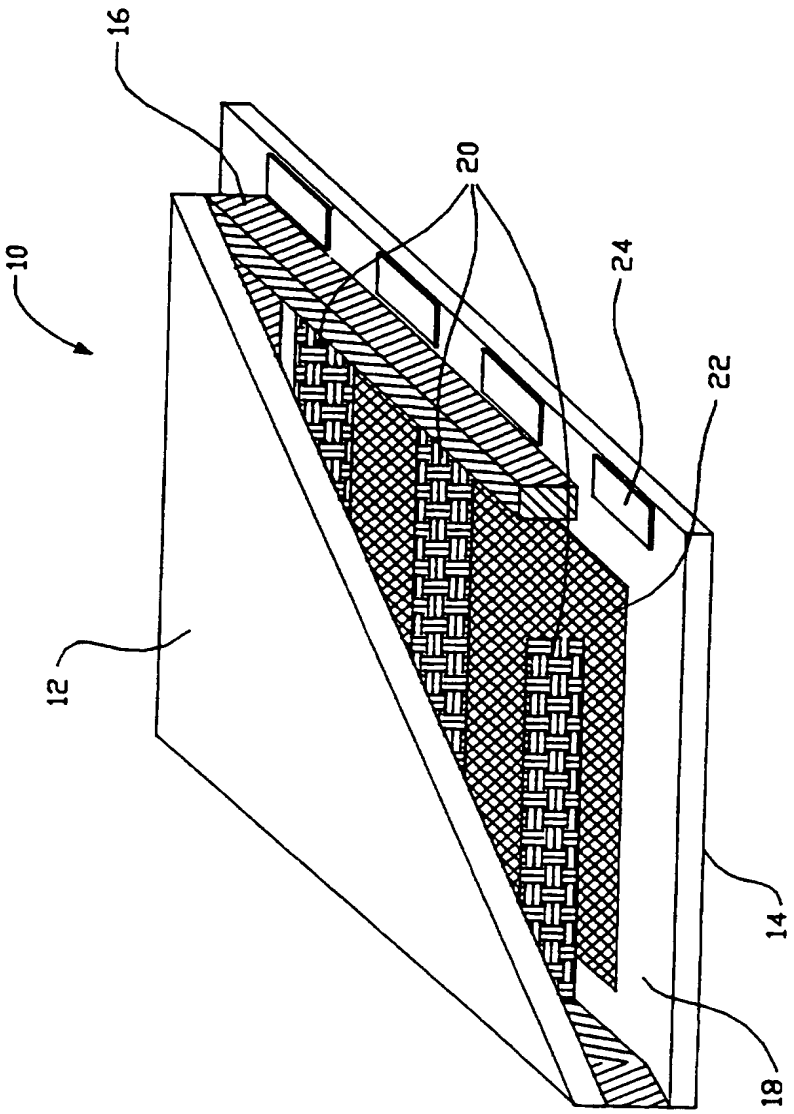


FIG.2

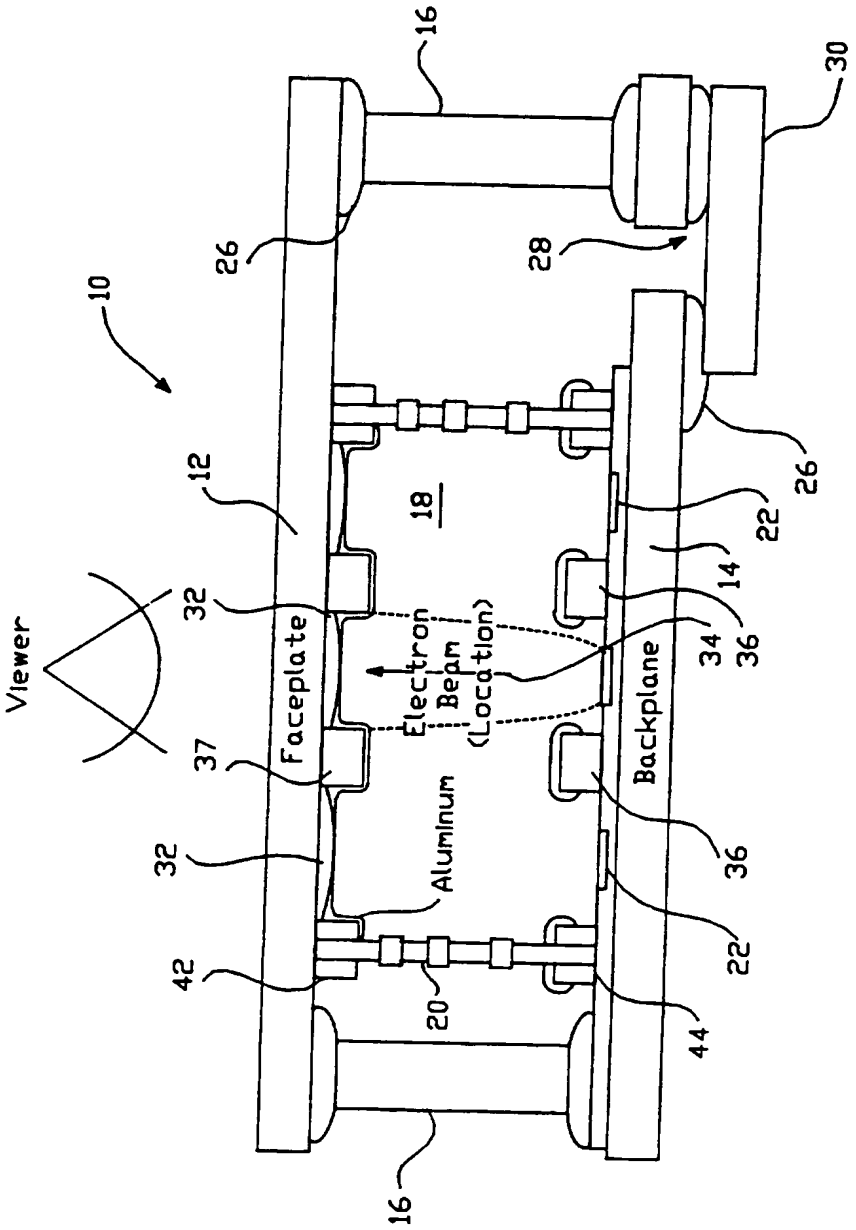

16
30
26
28
10
12
18
26
22
14
32
Viewer
Faceplate
Electron Beam (Location)
34
36
37
Backplane
Aluminum
32
36
22
42
20
44
16

FIG.3

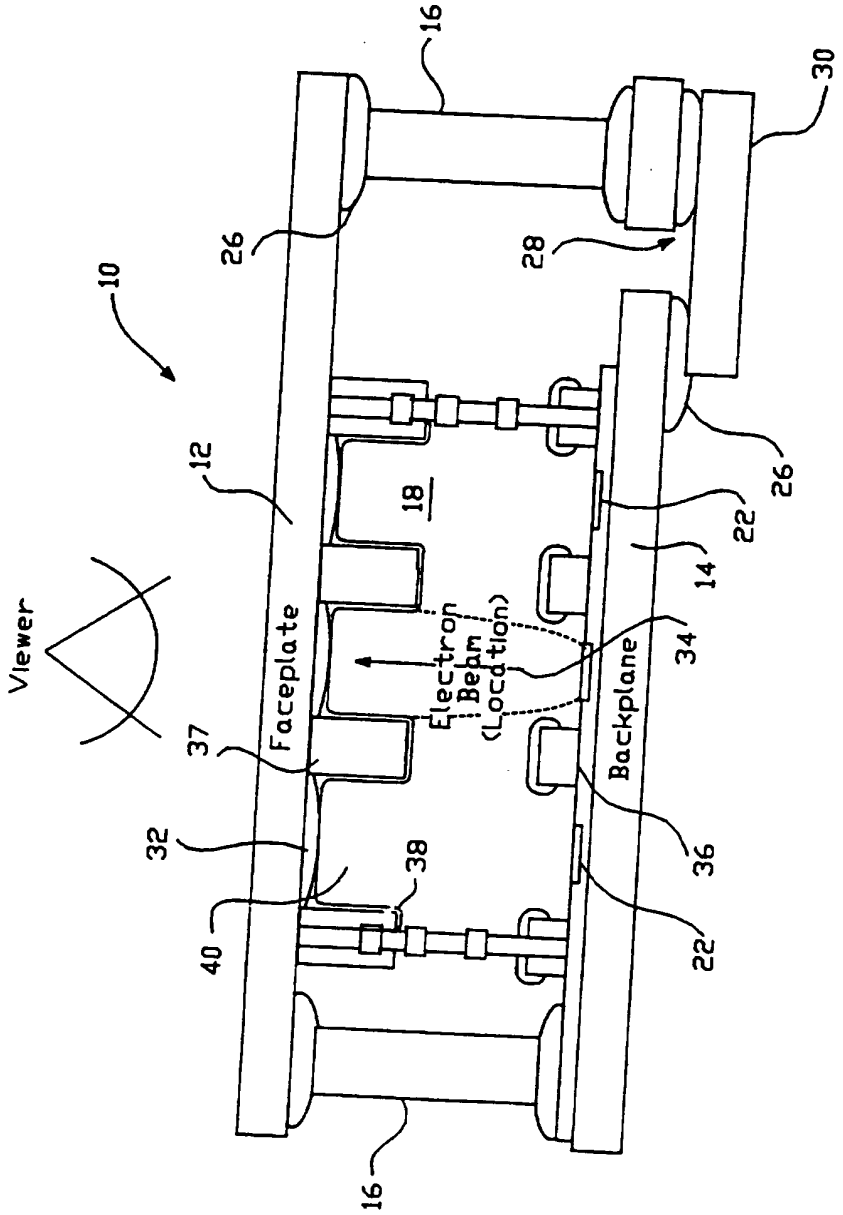

16
30
26
28
10
12
18
26
22
14
Viewer
Faceplate
Electron Beam (Location)
34
Backplane
37
32
38
36
40
22
16

FIG. 4

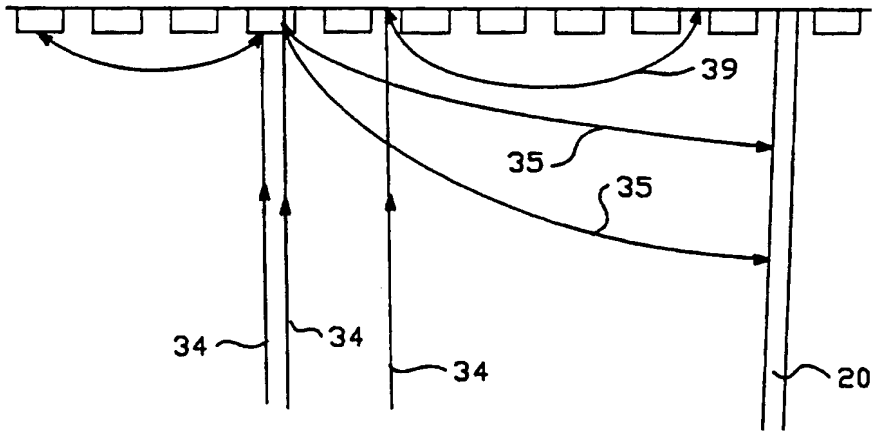


FIG.5

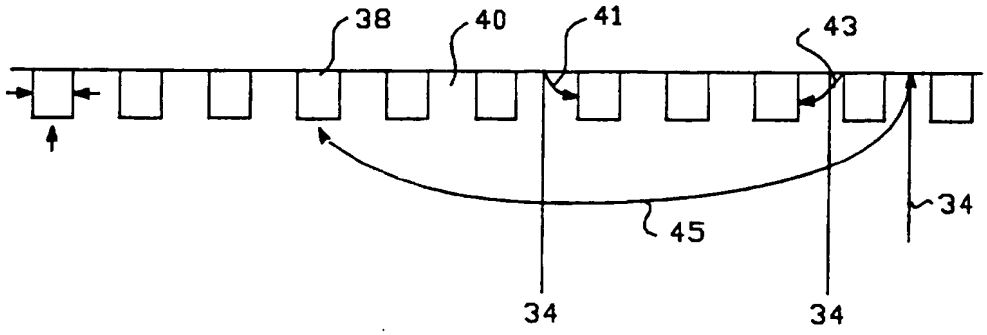
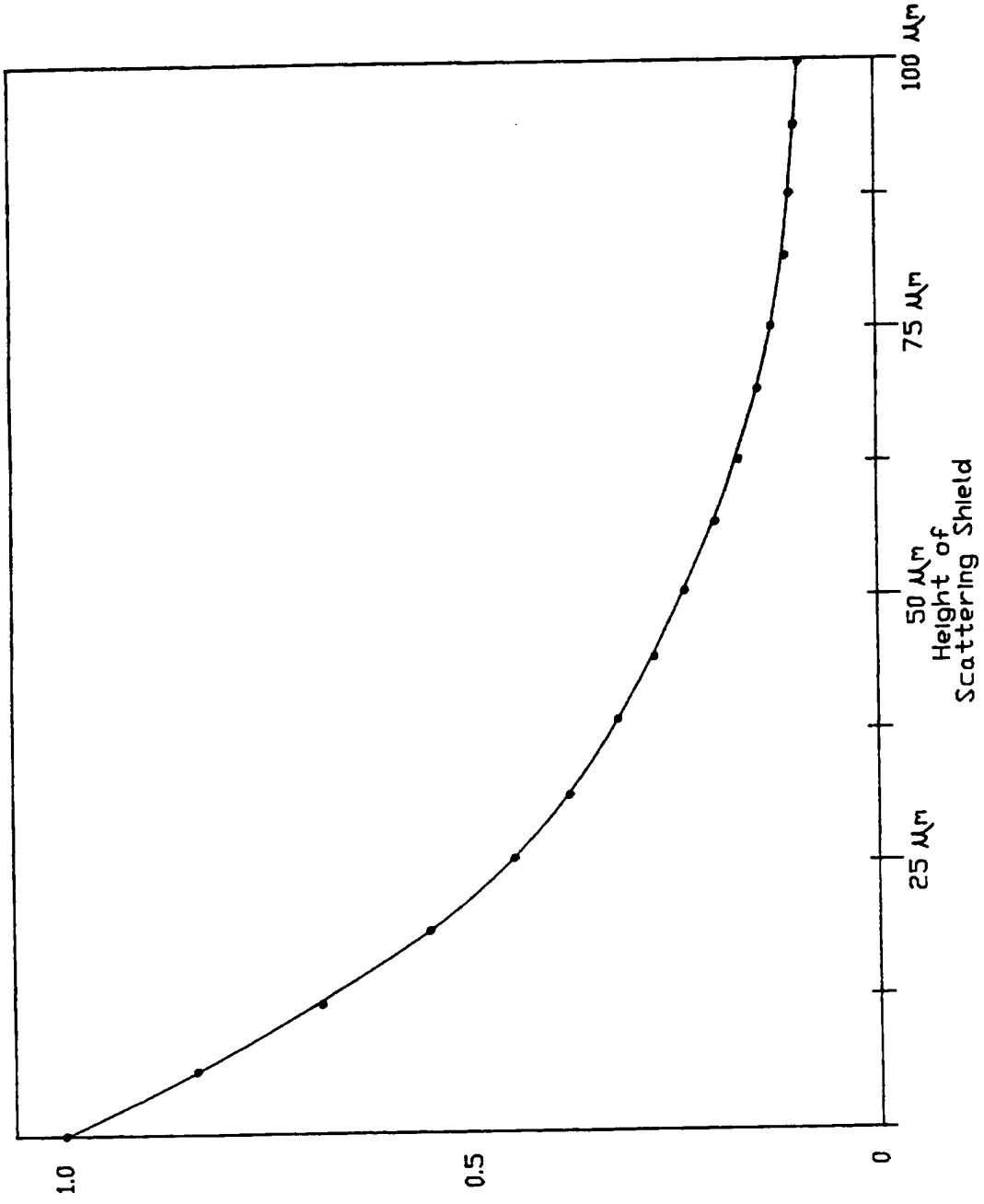


FIG.6

FIG. 7



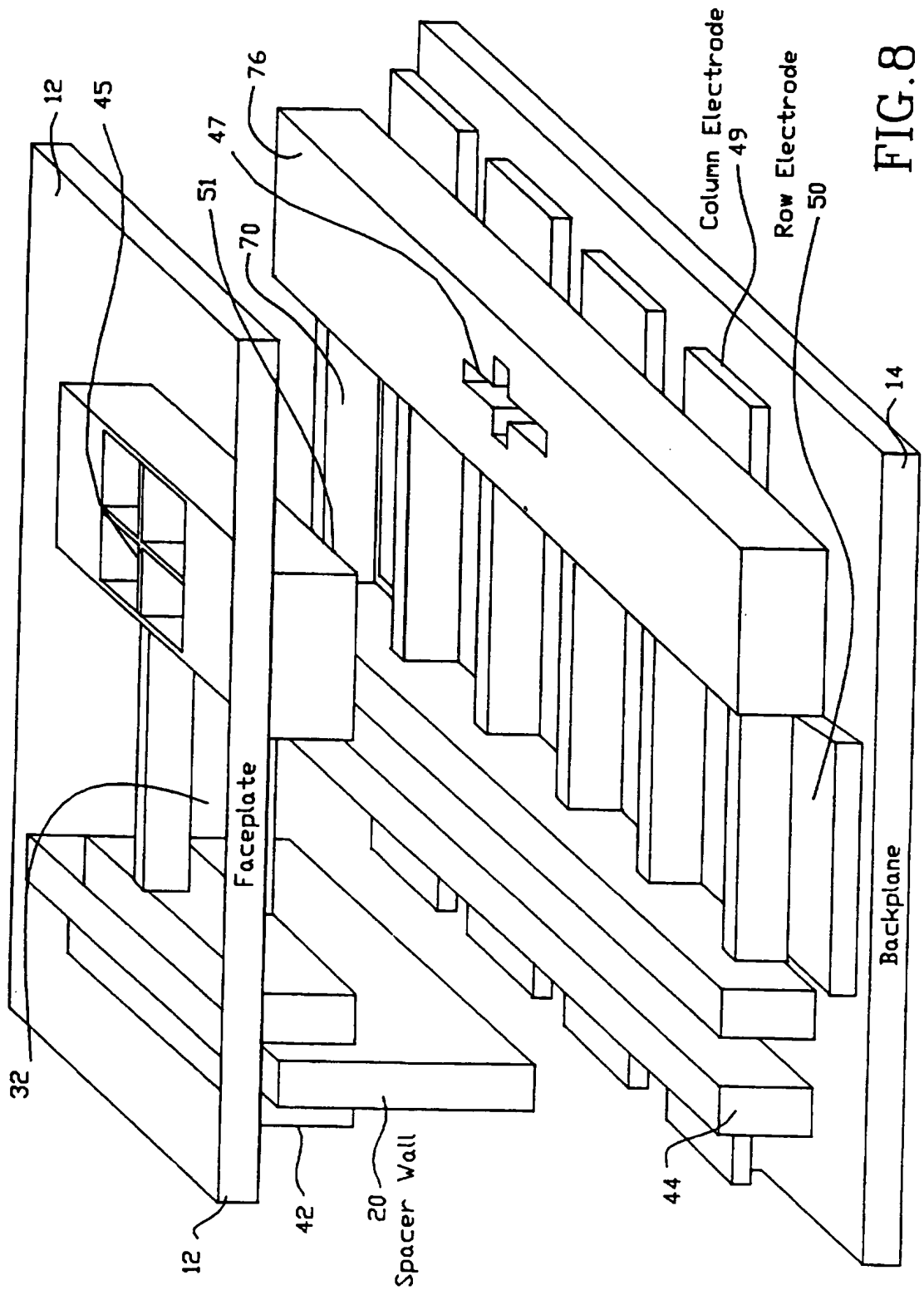

12
45
76
47
51
70
Column Electrode
49
Row Electrode
50
14
Faceplate
Backplane
32
42
20
Spacer Wall
44
12

FIG. 8

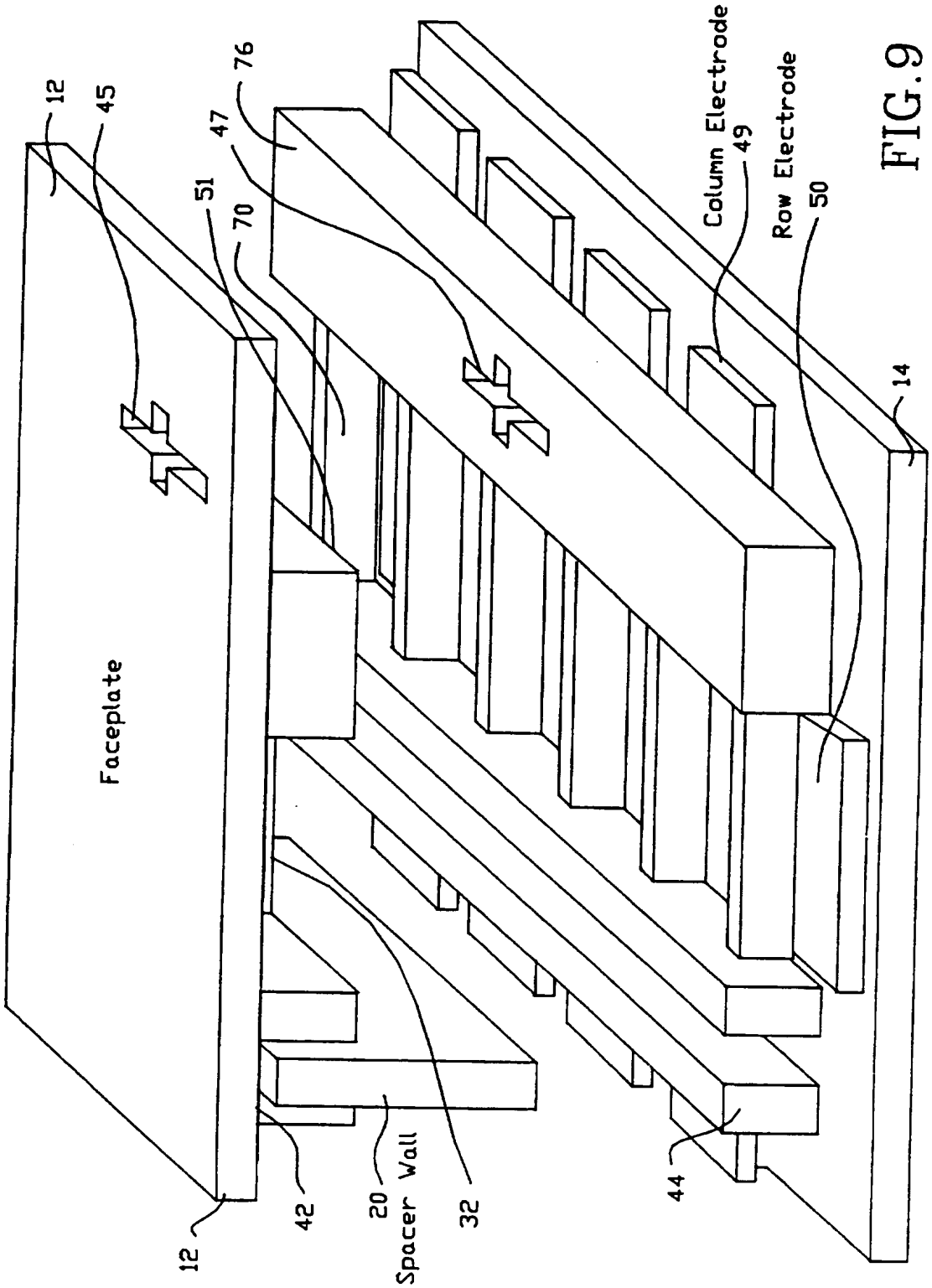
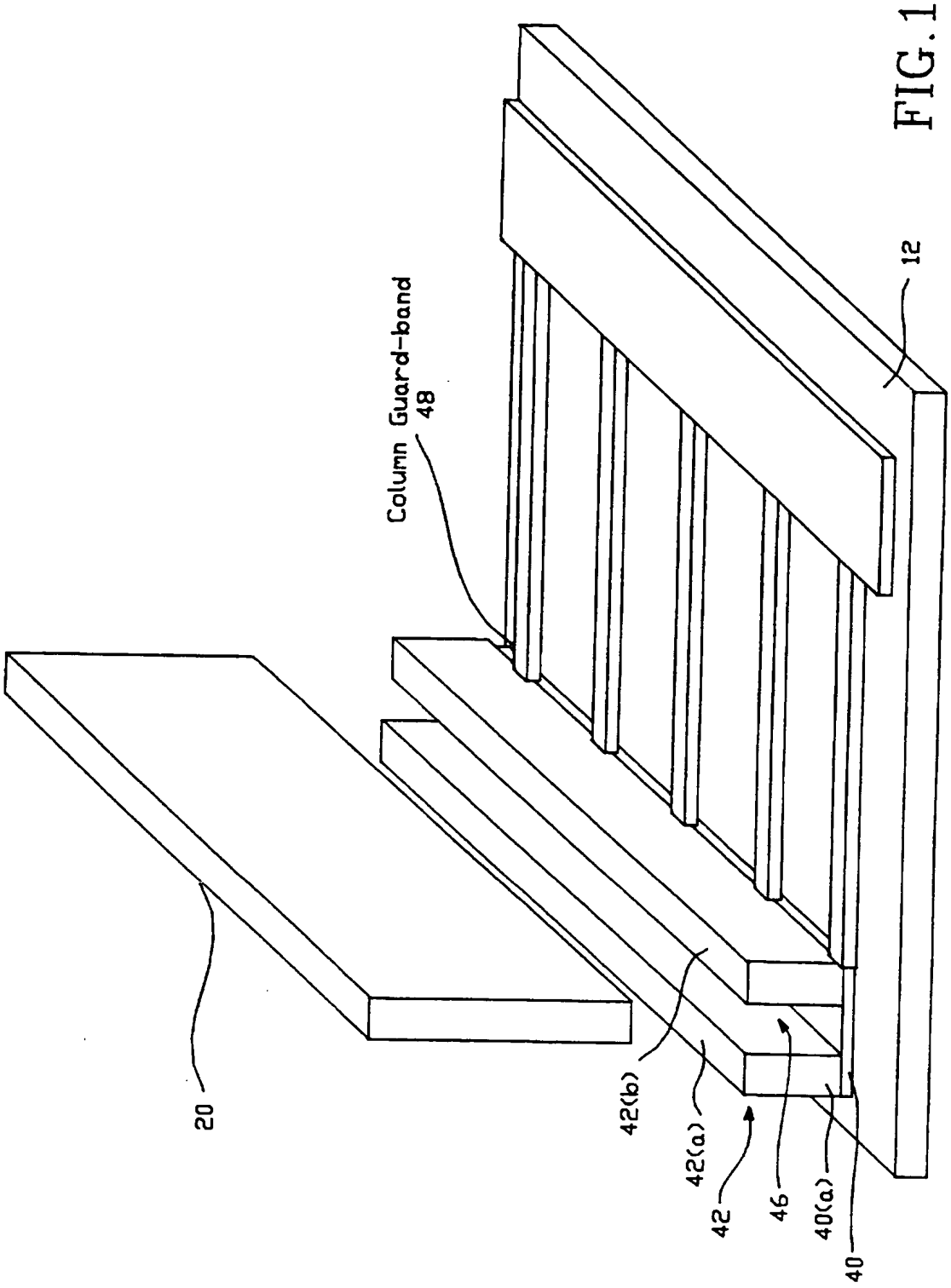

12
45
47
76
51
70
Column Electrode
49
Row Electrode
50
14
Faceplate
12
42
20
Spacer Wall
32
44

FIG.9

FIG.10



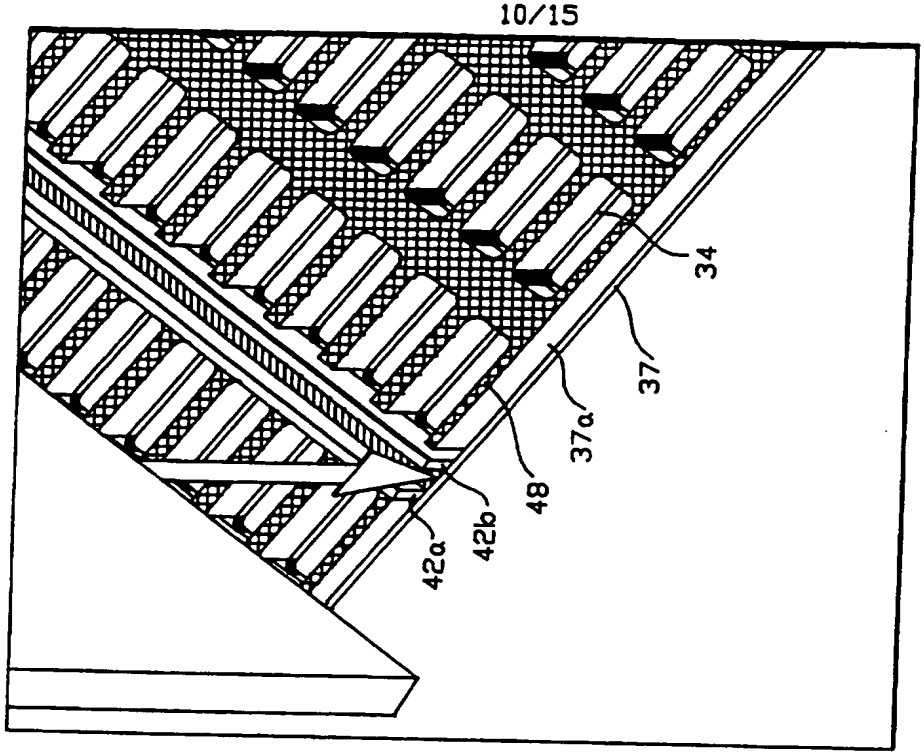


FIG.12

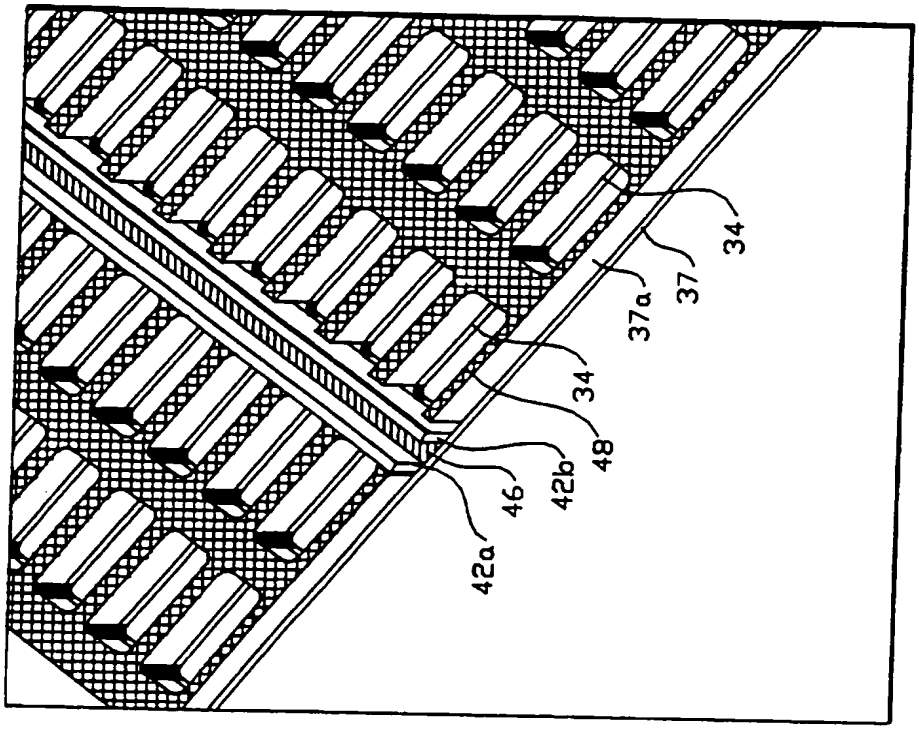


FIG.11

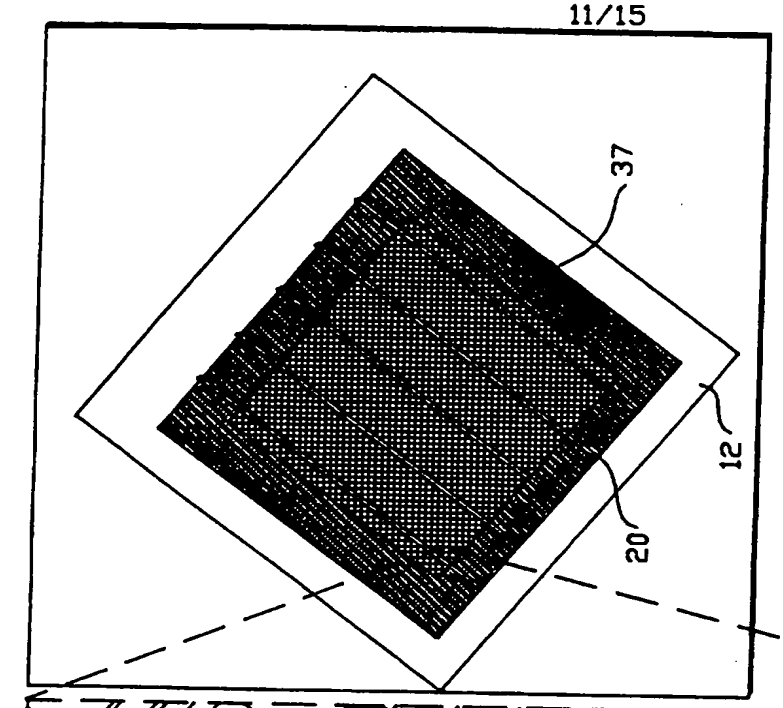


FIG. 14

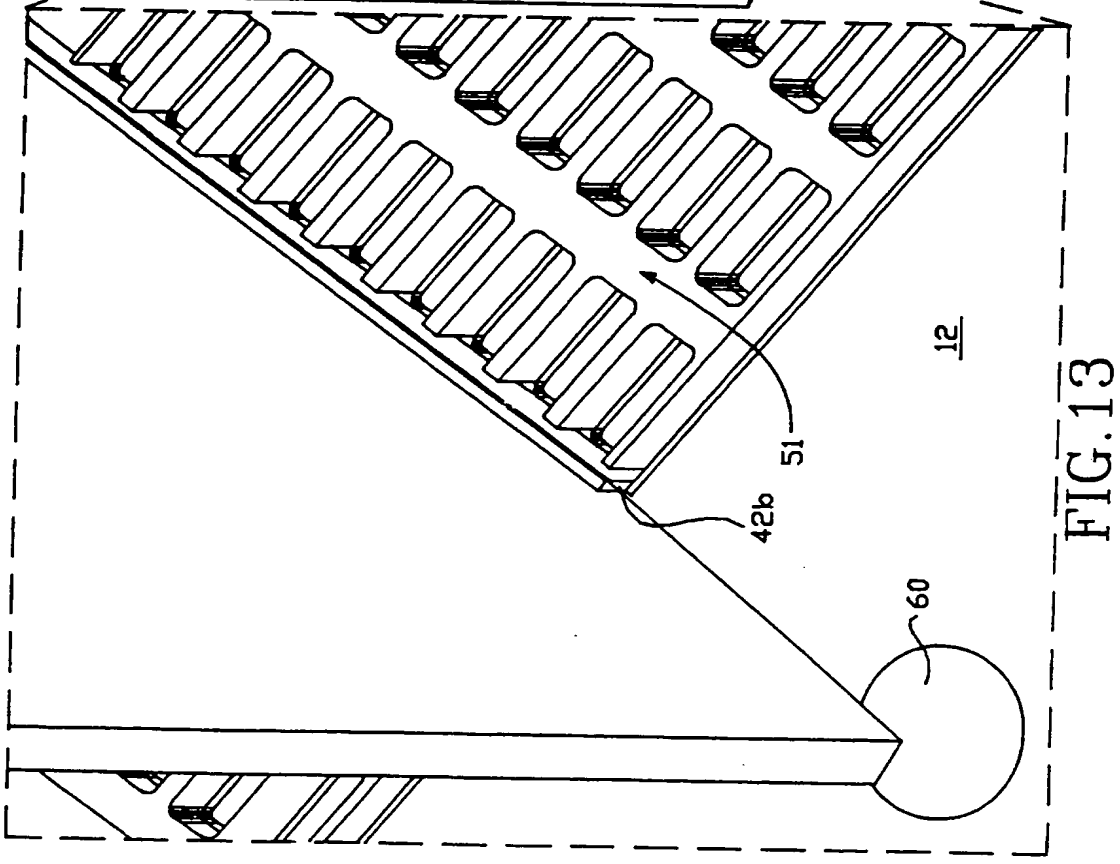


FIG. 13

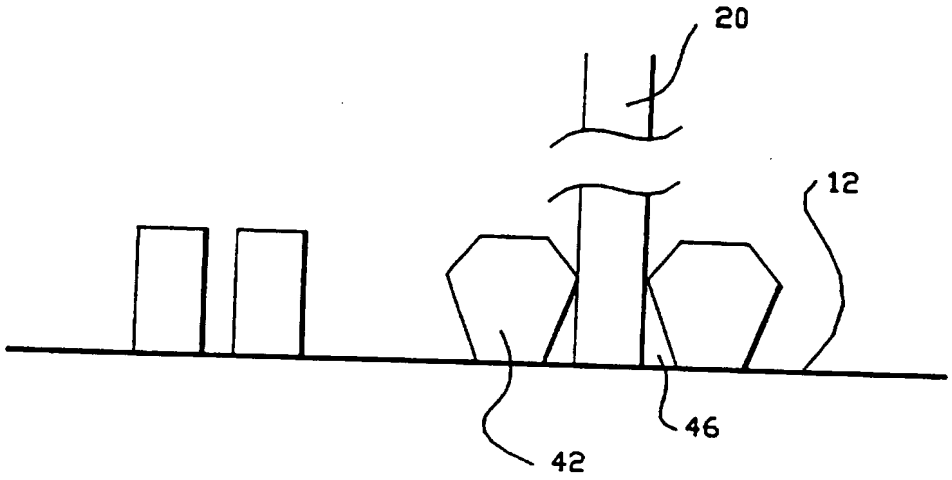


FIG. 15

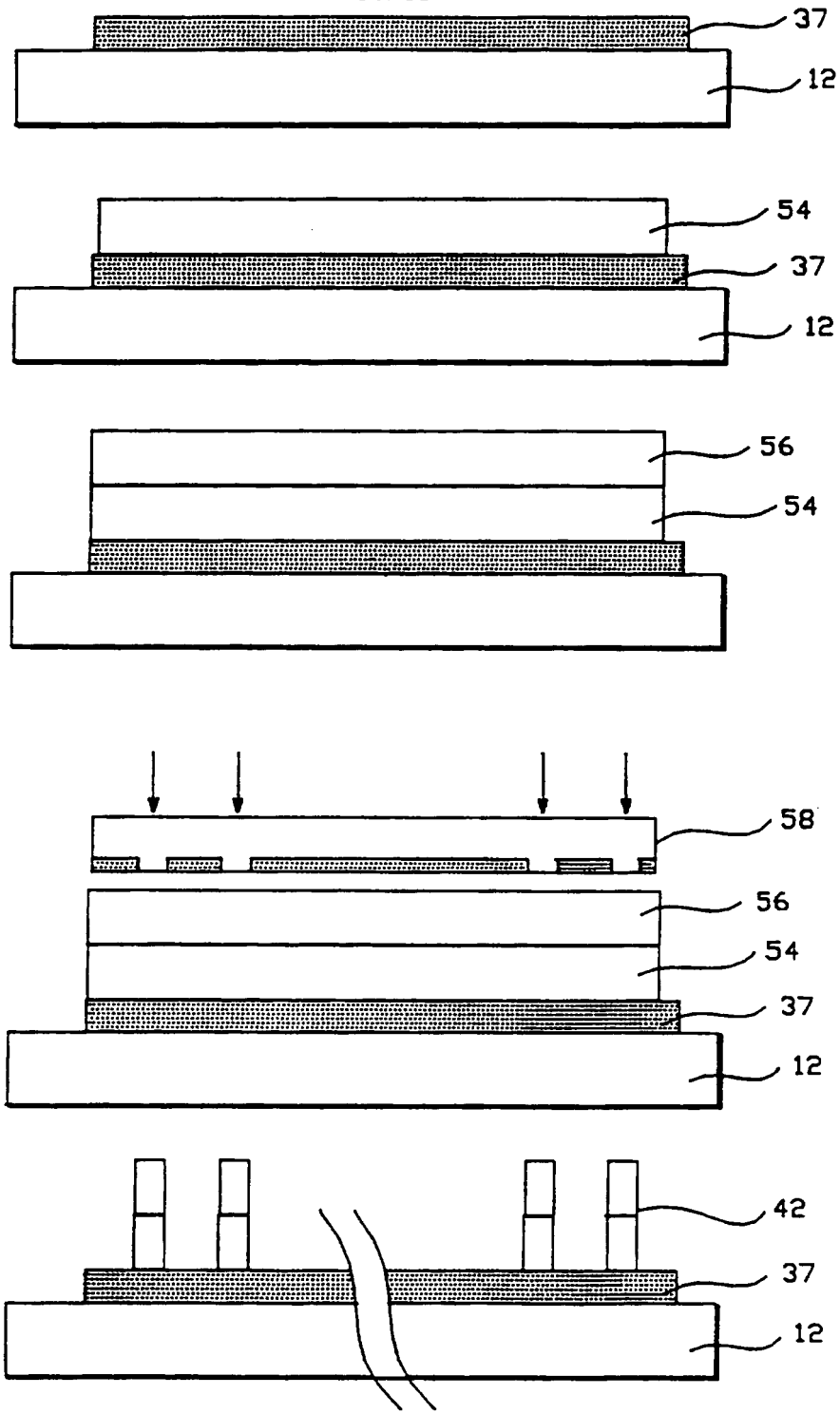


FIG. 16

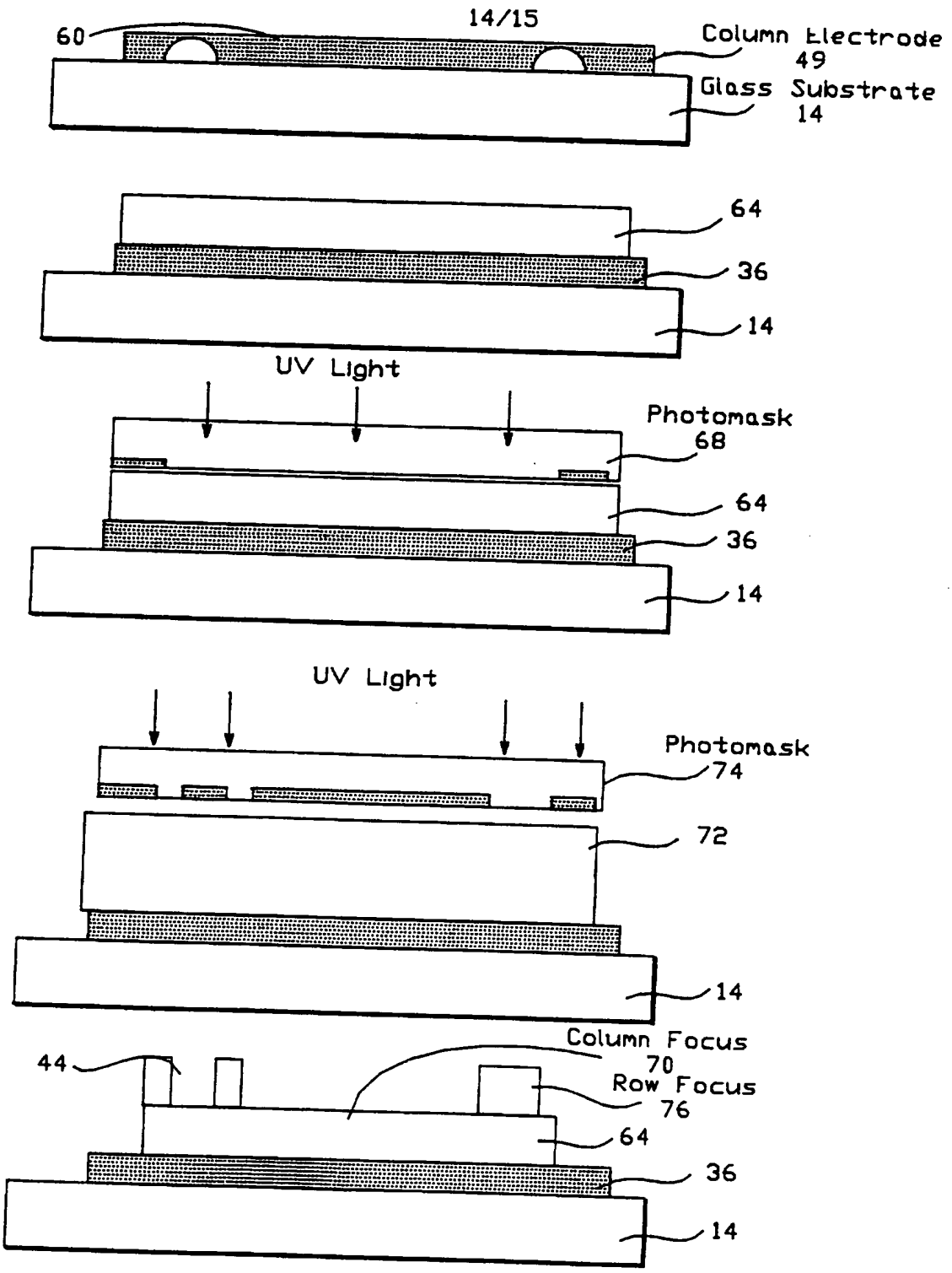

60
Column Electrode
49
Glass Substrate
14
64
36
14
UV Light
Photomask
68
64
36
14
UV Light
Photomask
74
72
14
Column Focus
70
44
Row Focus
76
64
36
14

FIG. 17

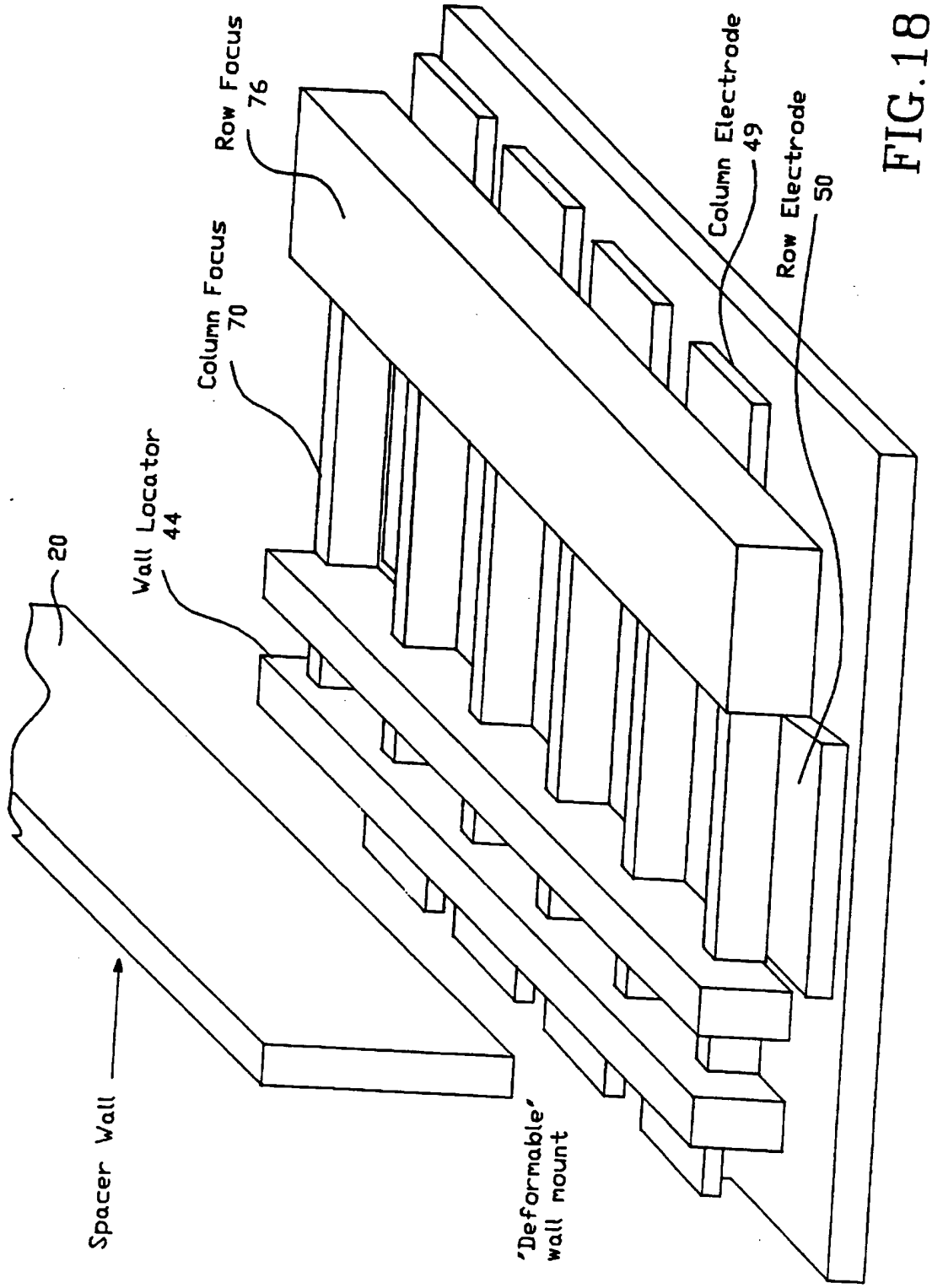

Row Focus
76
Column Focus
70
Wall Locator
44
20
Spacer Wall
'Deformable'
wall mount
Column Electrode
49
Row Electrode
50

FIG. 18

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08/343,803	21 November 1994 (21.11.94)	US

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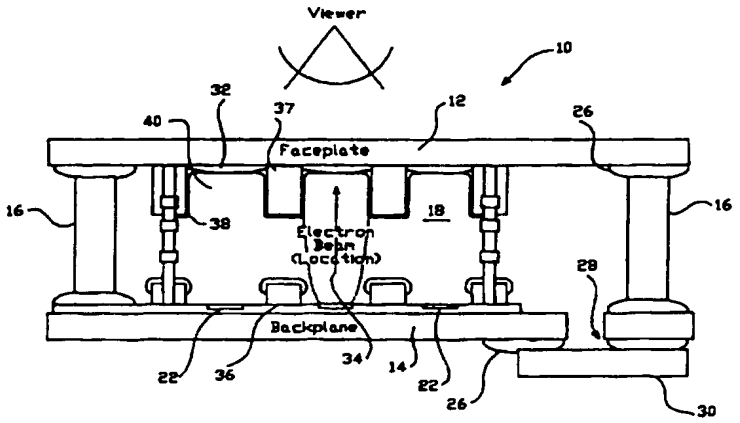
(54) Title: FIELD EMISSION DEVICE WITH INTERNAL STRUCTURE FOR ALIGNING PHOSPHOR PIXELS WITH CORRESPONDING FIELD EMITTERS



(57) Abstract

A field emission display device has a faceplate and a backplate. The faceplate includes a faceplate interior side with an active region made of a plurality of phosphor pixel elements; and the backplate has a backplate interior side with a plurality of field emitters. Sidewalls are positioned between the faceplate and the backplate, to form an enclosed sealed envelope between the sidewalls, backplate interior side and the faceplate interior side. At least one spacer wall in the envelope supports the backplate and the faceplate against forces acting in a direction toward the envelope. At least one internal structure fixes and constrains the faceplate and the backplate, and aligns a plurality of phosphor pixels with corresponding field emitters. Additonally, the faceplate can include at least one faceplate fiducial, and the backplate include a corresponding backplate fiducial. The faceplate fiductial is optically aligned with the backplate fiducial. First, the spacer wall is positioned in the wall gripper. The faceplate and backplate fiducials are then optically aligned, and the spacer wall then introduced into the locator. Phosphor pixels are aligned with their corresponding field emitters. There is no need for external fixturing devices in the high temperature bonding and sealing processes of the display.

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INTERNATIONAL SEARCH REPORT

Int. ional Application No
PCT/US 95/15226

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H01J31/12 H01J29/82

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H01J

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	EP,A,0 623 944 (AT & T CORP) 9 November 1994 see column 1, line 3 - line 5 see column 3, line 8 - line 36 see column 6, line 55 - column 7, line 24 see figure 5 ---	1-5
Y	WO,A,88 01098 (COMMTECH INT) 11 February 1988 see page 2, line 4 - line 17 see page 8, line 21 - page 9, line 6 see figures 2,3,5 ---	1-5
A	WO,A,94 15350 (MICROELECTRONICS & COMPUTER) 7 July 1994 see figure 5 see page 8, line 2 - line 17 see page 22, line 33 - page 23, line 26 --- -/--	3

[X] Further documents are listed in the continuation of box C. [X] Patent family members are listed in annex.

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1

Date of the actual completion of the international search	Date of mailing of the international search report
25 March 1996	07. 06. 96

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+ 31-70) 340-2040, Tx. 31 651 epo nl, Fax (+ 31-70) 340-3016	COLVIN, G

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INTERNATIONAL SEARCH REPORT

Int. ional Application No
PCT/US 95/15226

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	PATENT ABSTRACTS OF JAPAN vol. 011, no. 195 (E-518), 23 June 1987 & JP,A,62 022362 (MATSUSHITA ELECTRIC IND CO LTD), 30 January 1987, see abstract ---	10
A	WO,A,90 00808 (INNOVATIVE DISPLAY DEV PARTNER) 25 January 1990 see page 1, line 1 - line 5 see page 2, line 26 - page 3, line 5 see page 3, line 25 - page 4, line 12 see page 5, line 10 - line 15 -----	1,8

Form PCT/ISA/210 (continuation of second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

ernational application No.
PCT/US95/15226

Box I Observations where certain claims were found unsearchable (Continuation of item 1 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box II Observations where unity of invention is lacking (Continuation of item 2 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

1. CLAIMS 1-16,26-38 BLACK MATRIX ALIGNING STRUCTURE
2. CLAIMS 17-25,63-71 FOCUS ELECTRODE
3. CLAIMS 39-62 SCATTERING SHIELD

FOR FURTHER INFORMATION PLEASE SEE FORM PCT/ISA/206 MAILED 03.04.96.

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searches without effort justifying an additional fee, this Authority did not invite payment of any additional fee.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

1-16,26-38

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest.

☐ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/US 95/15226

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		DE-T-	68923074	19-10-95
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		JP-T-	3501547	04-04-91
		US-A-	5063327	05-11-91